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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,340	STOCKMEYER, LARRY J.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-23 and 27-35* is/are rejected.

7)☒ Claim(s) *8-10 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 33-35 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims refer to a "readable program code." This has been found to be able to include a written program code on paper or the like, which has been found to be non-statutory. The examiner suggests that this is reworded to say a "computer readable medium."

Claim Rejections - 35 USC § 103

3. Claims 1, 4-7, 11, 14-17, 20-23, 27 and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the background of the specification in view of "Interconnection Network Switch Design for Parallel DSP Systems" by Fujii et al.

4. As per claim 1:

A method of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of the partitions comprises the processing unit of at least one of the processors, and where L is an integer >= 2 and R is an integer >= 1 (Background of Specification).

The background does not teach connecting the L switches of the L processors among the external ports of the L switches in an extended torus architecture.

Fujii teaches that the advantages of an extended torus are already well known in the art, and that the layout can be used to process moving SHD images (Fujii: 2; 3.2).

Therefore it would have been obvious to one of ordinary skill in the pertinent art to organize the switches of the background of the specification in an extended torus architecture since it has many well-known advantages and can be used to process moving SHD images.

Fujii basically defines the extended torus as a 3-D tours. Therefore, setting the connected L switches, thereby interconnecting each of the partitions as a torus, would inherently flow from this.

5. As per claim 4:

The method of claim 1 wherein the connecting comprises:

connecting the L switches via cables (Specification 2, lines 4-6).

6. As per claim 5:

The method of claim 1 wherein the setting comprises:

computing the span of the partition (Specification 7, lines 7-10).

7. As per claim 6:

The method of claim 5 wherein the computing comprises:

finding the minimum coordinate, MIN, in the partition (Specification 7, lines 7-10);

determining the maximum coordinate, MAX, in the partition (Specification 7, lines 7-10); and

setting the span of the partition to be equal to the set of coordinates i, where MIN <= i <= MAX, where i is an integer (Specification 7, lines 7-10).

8. As per claim 7:

The method of claim 6 wherein the computing further comprises:

if the span of the partition contains exactly one coordinate, where i is the coordinate that belongs to the span, connecting the first internal port and the second internal port (I1,I2) of the ith switch (Specification 7, lines 29-31).

The background states that a partition that contains N coordinates, where N is at least 2, will use at least N external links. That means that a partition of 1 coordinate is an exception that will use no external links. According to the definition of a torus, the partition must complete a loop, so therefore, if the partition contains 1 coordinate and must complete a loop, the internal ports will inherently be connected.

9. As per claims 11, 14-17, 20-23, 27 and 30-35:

Claims 11, 14-17, 20-23, 27 and 30-35 recite the same limitations as claims 1 and 4-7 and are rejected for the same reasons.

The system claims teach an apparatus to perform the method of the method claims. This is inherent.

The computer program product claims teach a computer readable program code that contains instructions to execute the method of the method claims. This is inherent.

10. Claims 2, 3, 12, 13, 18, 19, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the background of the specification in combination with "Interconnection Network Switch Design for Parallel DSP Systems" by Fujii et al. as

applied to claims 1, 11 and 17 above, and further in view of Jackson et al. (US Patent 5,715,391).

11. As per claim 2:

Fujii does not teach the first external port switch 1 and the first external port of switch 2 or any of the actual connections between the switches in the 3-D torus architecture (extended torus) while Jackson does (Jackson: Figure 5A, item 506E).

Jackson uses the leapfrog torus geometry (Jackson: Figure 5A; column 3, lines 21-26). The leapfrog geometry eliminates the very long connection in a torus between the first and last node. This connection can increase latency.

Therefore it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Jackson to Fujii would eliminate the long connection between the first and last node in a torus geometry.

12. As per claim 3:

Jackson teaches the connections in the extended torus further comprising:

if L >= 3, connecting the fourth external port of the (L-1)th switch and the fourth external port of the Lth switch (Jackson: Figure 5A, item 506F);

for 1 <= i <= L-2, where i is an integer, connecting the fourth external port of the ith switch and the first external port of the (i+2)th switch (Jackson: Figure 5A, item 504G).

Jackson does not teach for 1 <= i <= L-1, where i is an integer, connecting the third external port of the ith switch and the second external port of the (i+1)th switch.

This constitutes mesh architecture which is taught by the background of the specification (Figure 1E).

The background of the specification states that the mesh architecture has the desirable property that every partition can be interconnected as a mesh (Specification, page 6, lines 24-26).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art to additionally have Jackson, for 1 <= i <= L-1, where i is an integer, connecting the third external port of the ith switch and the second external port of the (i+1)th switch to have every partition be able to be interconnected as a mesh.

13. As per claims 12, 13, 18, 19, 28 and 29:

Claims 12, 13, 18, 19, 28 and 29 recite the same limitations as claims 2 and 3 and are rejected for the same reasons.

The system claims teach an apparatus to perform the method of the method claims. This is inherent.

Allowable Subject Matter

14. Claims 8-10 and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 and 24-26 describe very specific connection schematics for the switches of the processing elements to correspond to the layouts of claims 2, 3, 18 and 19 in variant instances where N >= 2. While the background of the specification in

combination with "Interconnection Network Switch Design for Parallel DSP Systems" by Fujii et al. in view of Jackson et al. teach the layout described by the applicant, there is no way to anticipate how the internal connections would be done.

For instance, with respect to claim 8 where i=1, the connections of switch 1 could easily be (E1, I2) and (E3, I1).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Multiprocessor Networks: Message-Based Parallel Processing by Reed et al. teaches the advantages of an extended torus architecture.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
Art Unit 2183

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